Heat Transfer Engineering, 26(3):79–88, 2005

ISSN: 0145-7632 print / 1521-0537 online
DOI: 10.1080/01457630590907392

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Direct Comparison between Five Different Microchannels, Part 1: Channel Manufacture and Measurement

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This paper is the first in a two-part study of the pressure-flow characteristics for a range of microchannels. Here, the manufacture of the channels and the resulting quality in terms of the channels' closeness to target dimensions, channel-to-channel variation for each sample, and the difference in area between the assumed perfect rectangular/trapezoidal shape of the channels and their actual cross-section are addressed. Wet etching with KOH produced trapezoidal channels 577 μm wide and 413 μm high. DRIE produced rectangular channels 304 μm wide and 332 μm high. Mechanical sawing produced near rectangular channels in both silicon and plastic. The silicon channels were 52 μm wide and 423 μm deep, and the plastic channels were 203 μm wide × 344 or 382 μm deep. Channel dimensions were measured using a scanning electron microscope. This paper demonstrates the feasibility of producing relatively large microchannels in two materials by three methods.

The sustained drive toward faster, smaller, and more complex silicon devices has led to a considerable increase in the power density of modern processor chips. At present, cost performance/high performance devices cannot operate reliably at junction temperatures greater than 90°C [1]. The International Technology Roadmap for Semiconductors (ITRS, 2003) also predicts this figure to drop to 85°C by 2005. The maximum ambient temperature at which these devices should reliably operate is 45°C, giving a mere 40°C temperature drop across which 80 W must be dissipated. These requirements necessitate the design of cooling systems with higher heat transfer coefficients and lower thermal resistances than are currently available. To put this in perspective, the ITRS (2003) states that the power density of the processor chip in a modern computer is 570,000 W/m^2. In comparison, a space shuttle can experience heat fluxes of 80,000 W/m^2 during re-entry. The power density in silicon processors is predicted to increase by an average of 6% per year until at least 2009 [1].

Many thanks to Joe O'Brien (NMRC) and Susan Deane (NMRC) for their help with the manufacturing processes. Thanks also to Paddy O'Regan (UL) for his assistance in the construction of the test system.

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The use of microchannels to cool silicon devices was first proposed using wet etched silicon channels [2]. Since then, other methods have been used, including deep reactive ion etch (DRIE) [3], electroplating [4], precision sawing [5], electro-discharge machining [6] CNC milling [7], and LASER ablation [8].

More recent work [9] describes the use of advanced DRIE techniques to create features of multiple heights on the floor of microchannels, potentially further enhancing heat transfer. The purposes of this study are to manufacture constant cross-section channels using a number of these methods and rate the suitability of these methods for manufacture and performance as part of a silicon device. Part two of this paper will be devoted to describing the test system and measuring the flow through the manufactured channels.

This work describes the manufacture of a variety of comparable microchannels using diverse methods. To allow the channels to be compared, all the channels are cut in the surface of 16 × 30 mm rectangular pieces. Since the area of each piece is the

same, a test system can be built that uses the same inlet and outlet manifolds, as well as the same data acquisition system to test each channel.

It was decided that, if possible, all of the channels should have a glass cover bonded over them in order to allow optical access to the channels so that trapped air bubbles or other unexpected blockages can be spotted. Bonding a cover over the channels also ensures that no flow can pass over the tops of the channel walls. Some theoretical work has shown that leaving a gap over the walls increases the heat transfer from microchannels under constant pumping power [10], but practical control of this gap is difficult.

The manufacturing methods used were developed and carried out in the NMRC, Ireland. The processes used were precision sawing of plastic, silicon and glass; DRIE; and KOH etching. The experimental apparatus that has been made to test these samples uses the same inlet and outlet manifolds, pressure tappings, and thermocouples to test each channel. It is built using as many standard parts as possible, allowing it to be dismantled and rebuilt easily as well as allowing the whole system to be rearranged if necessary.

As can be seen from Figure 1, the sample (4) fits into the shim (5), which then fits into the manifold block (6). Because the samples are available in a variety of thicknesses, several shims have been made with grooves of different depths. The result of this is that all the channel samples, when fitted in their corresponding shims, occupy the same volume. Since the only change in the flow system from sample to sample is the size of the channels being tested, the effects of different manifolds, pressure tapping locations, and thermocouple locations are eliminated even though totally different channels are being tested.

PLASTIC MANUFACTURING PROCESS

The plastic channels were made from two different thermoset plastics, referred to in this paper as plastic 1 and plastic 2. Since these are both used in industry for the encapsulation of silicon devices, it makes sense to investigate their thermal performance, as channels could potentially be embossed onto the chip encapsulation far more cheaply and easily than they could be etched into the silicon chip, and with a lower thermal resistance than a heat sink clamped onto the encapsulated chip.

The plastic samples were made by injecting plastic into an empty 35 mm BGA mold, causing contamination to be left on the sample (see Figure 2a). This is removed with light emery paper. The sample was then mounted on a silicon wafer using wax (b). This allows a standard vacuum chuck to hold the sample in position during cutting.

The dicing saw used is a Disco Automatic dicing saw DAD-2H/6T. Prior to use, the saw calibrates itself by touching the blade off the chuck on which the sample sits. This allows wear in the blade and different blade diameters to be compensated for, and gives a zero from which the cutting depth can be set.

Cutting was performed using a plastic specific blade. A thin layer of spray paint had to be applied to the surface of the sample in order to allow the optical alignment of the sample with the blade to take place.

After cutting, the remaining paint was polished off the surface of the sample using a Logitech PM2 Precision Polishing Machine and 3 micron diamond paste. This leaves a clean flat surface for the glass to be bonded over. Any remaining wax from the mounting process is melted off on a hotplate or dissolved in an acetone bath at 70°C.

A 100 mm (4″) glass wafer is diced into pieces the same size as the plastic samples using a resin bonded diamond blade (f). A layer of photoresist is spun over the glass (g). SU-8-5 is the resist used. This is an epoxy-based negative photoresist that can be cured under UV light.

The glass and plastic are heated to 70°C on a hot plate. The glass pieces are then aligned and pressed into position over the plastic samples. Point pressure is applied by rolling a clock glass over the surface of the glass to create an initial bond. The partially bonded samples are then exposed to UV light. This starts

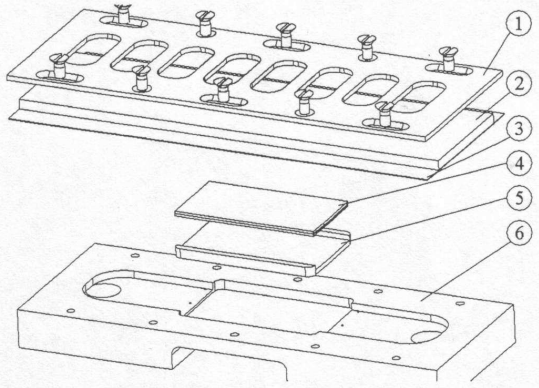


Figure 1 Layout of the microchannel tester.

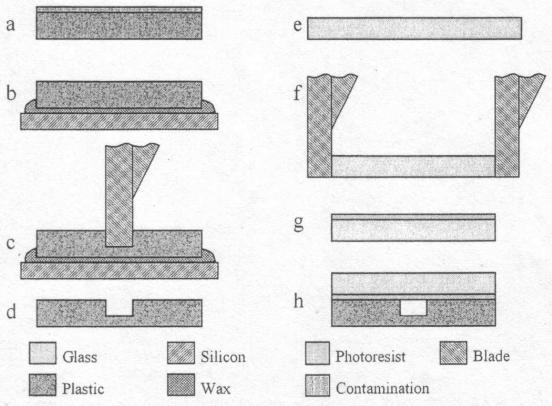
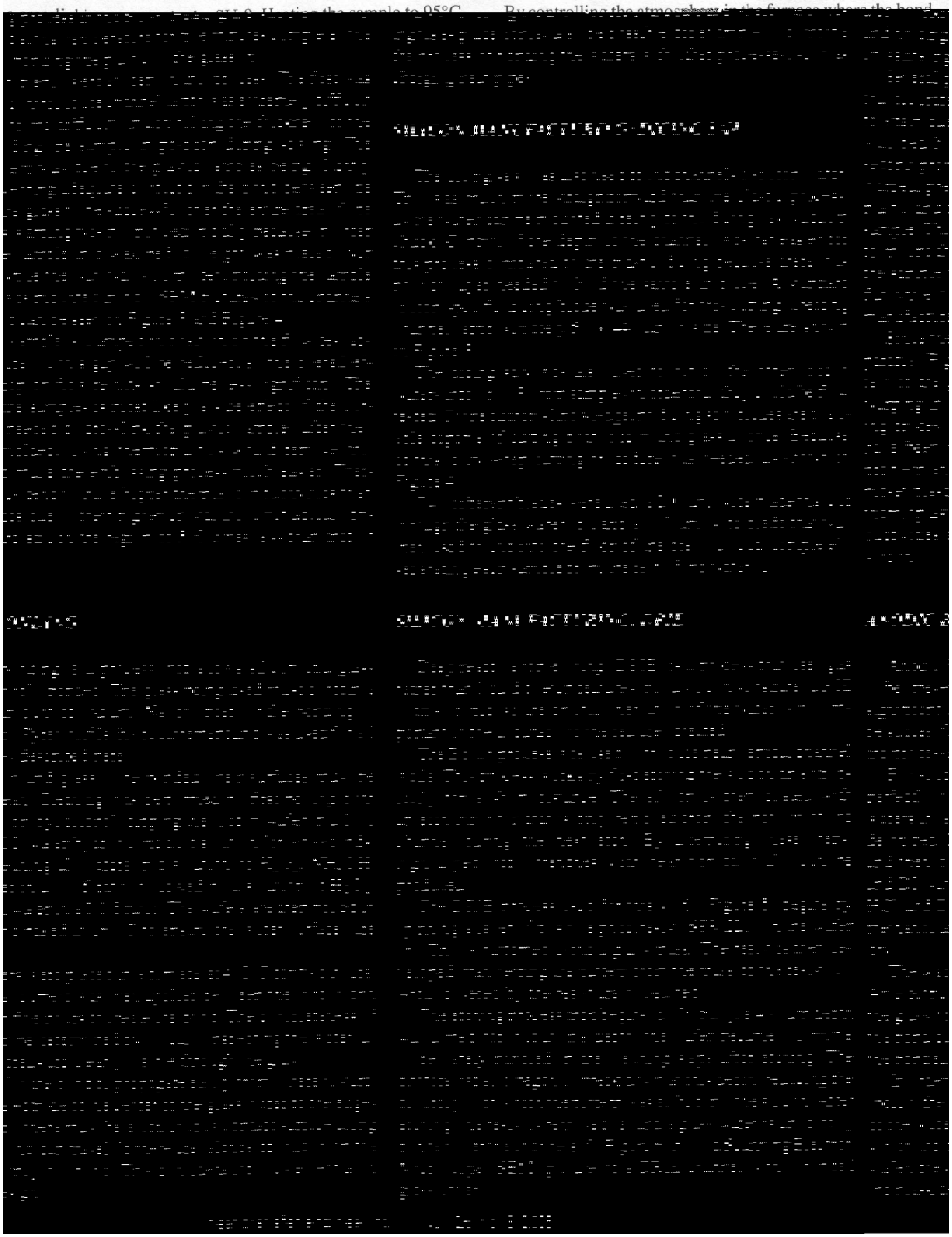


Figure 2 Processing steps in the manufacture of plastic channels.



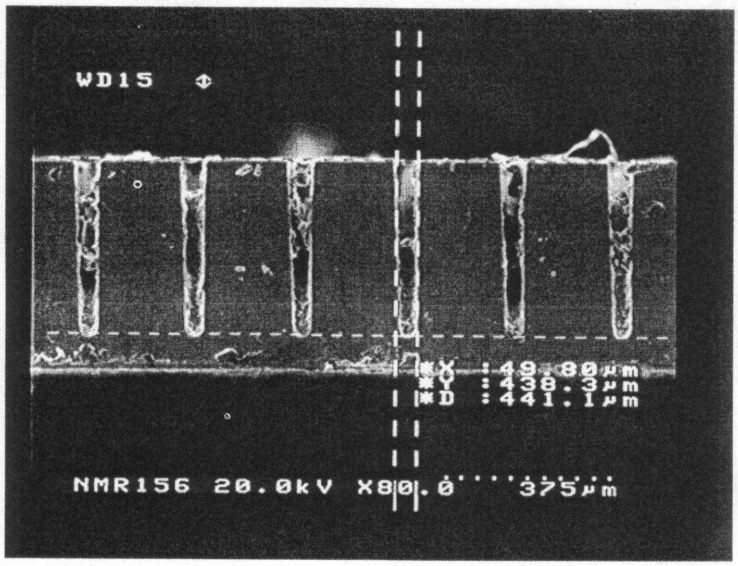


Figure 3 Diced silicon wafer. Contamination is due to handling outside clean room environments and chips remaining from the dicing process.

SILICON MANUFACTURING: KOH ETCHING

Potassium hydroxide (KOH) etching was also used to etch channels into a 100 mm (100) silicon wafer. KOH etches through (100) planes approximately 30 times as quickly as (111) planes. This results in trapezoidal or triangular channels, depending on the etch duration. The wall angle of the channels can be calculated using Eq. (1), where the Miller Indices of the planes are *(abc)* and *(xyz)*. For the KOH etch described here, the wall angle is 54.74°.

$$\theta = \cos^{-1}\left(\frac{ax + by + cz}{\sqrt{a^2 + b^2 + c^2} \times \sqrt{x^2 + y^2 + z^2}}\right) \quad (1)$$

Since the etch stops at the (111) planes in the silicon, a misalignment between the details on the mask and the (111) planes will produce stepped channel walls. For this reason, an alignment etch as described in [11] must be used. This etch uses a mask with 50 μm diameter circular holes that etch silicon in KOH to form pyramid shaped pits. The sloped walls of these pits follow the (111) planes in the wafer, allowing the channel mask to be correctly aligned.

The wet etch process (Figure 7) begins with a wafer clean followed by the growth of furnace oxide on the surface of the wafer (b). A chemical vapor-deposited nitride layer, resistant to the KOH solution, is deposited over the oxide (c). Photoresist is spun over the nitride layer and patterned using the alignment mask (d, e).

After the resist has been developed, a plasma etch is used to remove the exposed nitride (f). The photoresist is then removed (g). A sulphuric acid bath is used to remove the exposed oxide (h) and the alignment marks are KOH etched to a depth of 14 microns (i).

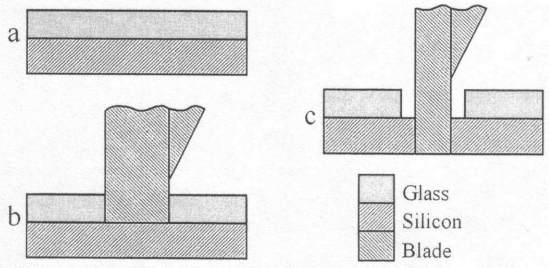


Figure 4 Two step dicing process.

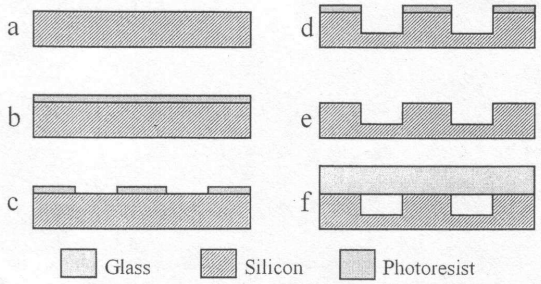


Figure 5 DRIE process including anodic bonding of a glass wafer onto the etched silicon.

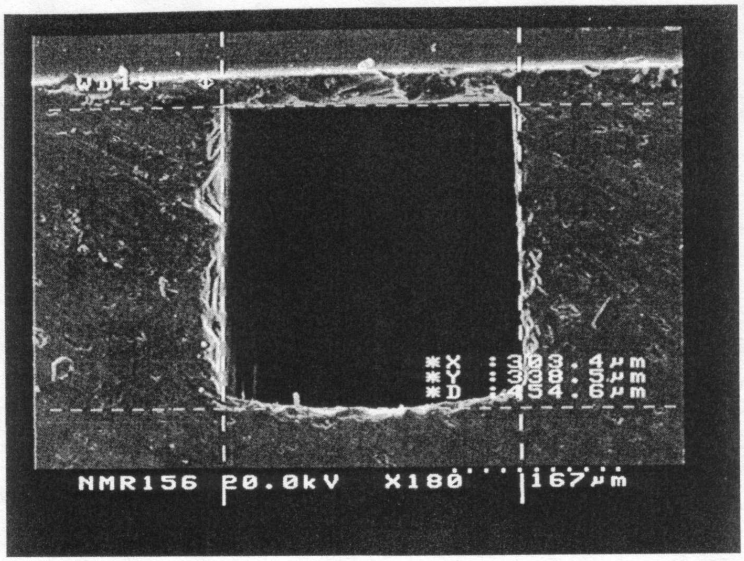


Figure 6 DRIE channel. Damage visible around the channel and the step in the glass over the channel are due to the dicing process.

The etch marks are then inspected, a new resist is spun over the surface of the wafer (j), and the mask with the channel details is placed over it and aligned to the etching marks already on the wafer. The etching process as described previously is then repeated producing etched microchannels (k–p). Etch depth is controlled by carefully measuring the etch duration as the etch rate is already known. The oxide and nitride are then removed (q). Finally, a glass wafer is anodically bonded over the silicon wafer (r), and the wafer is diced using the two-step process. The resulting channel can be seen in Figure 8.

CHANNEL MEASUREMENTS

The most significant source of error in matching the theoretical performance of channels with their experimental performance is that of measuring the size of the channel. This is why careful measurement of the dimensions of the channels is fundamental to correlating theoretical calculations for both pressure drop and heat transfer with measurements made.

Equation (2) shows the relationship between the pressure drop and the hydraulic diameter for a constant channel length

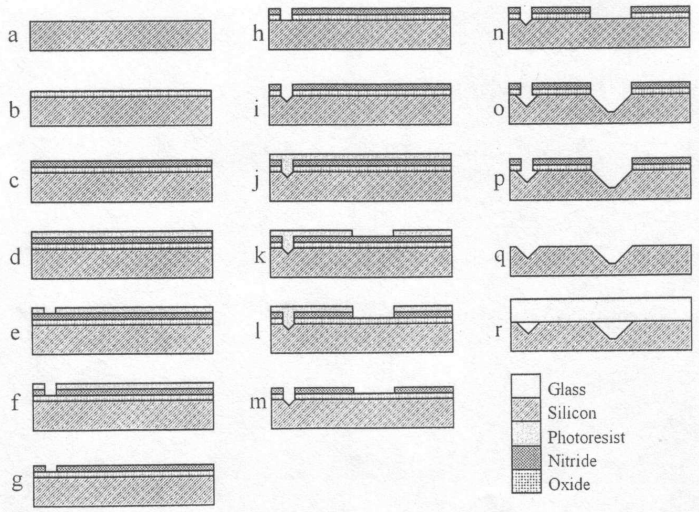


Figure 7 Wet etching process. Note the use of the same oxide and nitride layers for both etches in order to reduce the number of process steps.

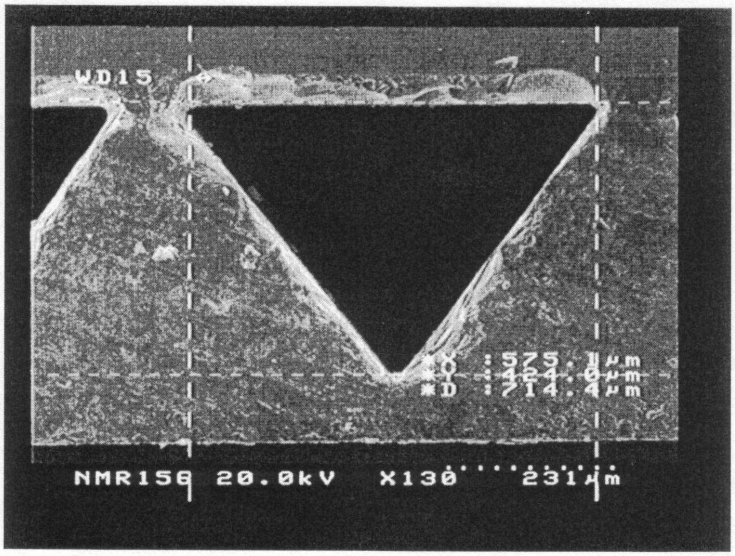


Figure 8 Wet etched trapezoidal channel with anodically bonded Pyrex cover. Etch was stopped when the channel was just short of being triangular.

and mass flow rate. The reason that the measurement of the channels is critical is because a small change in D_h will lead to significant changes in the pressure drop due to the high power to which D_h is raised.

$$P_L \propto \frac{1}{D_h^4} \tag{2}$$

The channels were measured using a scanning electron microscope (SEM), calibrated monthly to $\pm$ 0.3 µm on a 10 µm measurement. This allowed direct vertical and horizontal measurements to be made on the channels and produced photographs of the channels.

A program called DataThief (Tummers et al., 1999) was then used to take scaled points from the SEM pictures (see Figure 9). These points were exported as text to ProEngineer, a CAD program by the Parametric Technology Corporation (PTC), where they were used to create a 3D model of the channel cross-section. By analyzing the model, more accurate measures of the cross-sectional area and hydraulic diameter of the channel were calculated.

It should be noted that since the cross-section of the channel can't be assumed to be constant along its length, the measurements taken above only allow a comparison to be made between the accuracy of the overall width and height for an idealized

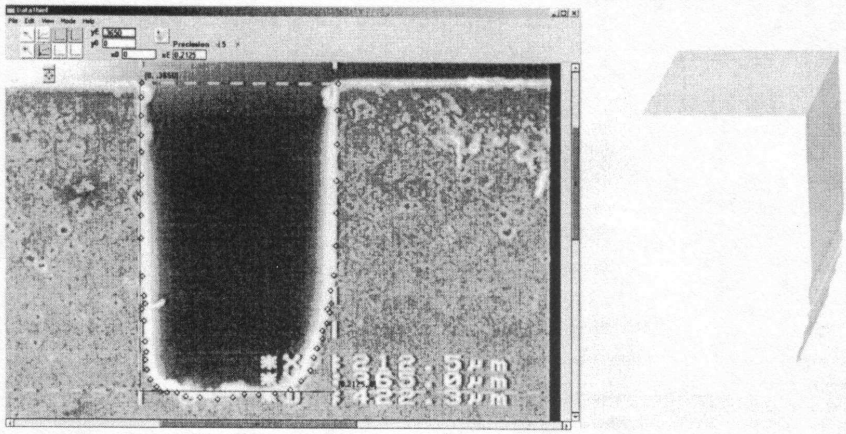


Figure 9 SEM photograph of a channel cut in Plastic 1, with overlaid data points on the left and a CAD model of the channel made using these points on right.

Table 1 Comparison between the target channel dimensions and the actual dimensions produced by each process

	Wet etched (trapezoidal)		Diced silicon		DRIE		Plastic 1		Plastic 2	
Manufacturing method	Target	Actual	Target	Actual	Target	Actual	Target	Actual	Target	Actual
Width (mm)	0.585	0.577	0.05	0.052	0.3	0.304	0.2	0.202	0.2	0.203
Height (mm)	0.4	0.413	0.4	0.423	0.32	0.332	0.4	0.344	0.4	0.382
CSA (mm^2)	0.1209	0.126	0.0200	0.022	0.0960	0.101	0.0800	0.073	0.0800	0.078
% Difference width/height	−3.25%	+1.37%	−5.75%	−4.00%	−3.75%	−1.33%	+14.0%	−1.00%	+4.50%	−1.50%
% Difference CSA	+4.50%		+9.07%		+5.04%		−8.95%		−2.87%	

rectangular channel as measured by the SEM and a more accurate model of the channel made from points taken from the same picture. Channel measurements were only taken through one plane for each sample.

RESULTS

The following tables contain a summary of the results recorded. Table 1 shows a comparison between the target dimensions of the channels for each manufacturing method and the actual dimensions measured for each process. Table 2 contains the averaged dimensions of each channel, the number of channels measured in each sample, and the sample standard deviation of the measured channel sizes for each process. Every third channel was measured on the diced silicon samples, and all channels were measured for the other four samples. Table 3 compares the results from single channels, which are assumed to be perfectly rectangular or trapezoidal, with a CAD model of the actual cross-section of the particular channel from a SEM photograph. The measurements that assume the channel to be perfectly rectangular or trapezoidal go toward the average dimensions in Table 2.

DISCUSSION

The data in Table 1 compare the expected dimensions for each channel with the actual dimensions measured for each channel. It can be seen that all processes are well within 10% of the target dimensions in terms of cross-sectional area (CSA).

For both the wet etch and DRIE processes, there was no way to check the depth of the channels while they were being processed, as the depth is a function of the etch time. The features etched using these processes are deeper than most of the etches performed in the NMRC, so it's understandable that the estimates of depth were slightly out. Both processes still produce channels that only deviate 5% from the target channel size.

For the dicing processes, changing the blade height in the saw controls the cutting depth. The error in the final depth of the diced silicon channels is most likely due to either the plastic film on which the wafer is stuck being thicker than expected or vibration in the blade as it cuts. The silicon wafer thickness was measured with a micrometer to be 525 ± 1 μm thick. This is equal to the supplier's quoted thickness.

There was far more variation evident in the depth in the diced plastic samples. This is due to a lack of repeatability in controlling the thickness of the wax layer between the silicon wafer and the plastic sample. Both plastic samples were intended to have the same dimensions, but instead there is a difference of almost 40 μm in their depths.

The 2.87% correlation between the target channel size and the actual size of the channels in plastic 2 (see Table 1) is not an indication that the process is repeatable. Separate test cuts, intended to be 600 μm deep in another sample of the same plastic, turned out to be 439 μm deep instead, showing the level of variation potentially present in the process. All of the diced channels tested here are two or three microns wider than the nominal size of the blades used to cut them. This difference is likely to be the contribution of vibration to the width variation in the channels.

Table 2 SEM measurements of five sets of microchannels (95% confidence interval [CI] = average value ± 2 × sample standard deviation): Size comparison between channels on the same sample. Low % deviation means all channels are similar in size, indicating process consistency

Manufacturing method	Wet etched (trapezoidal)		Diced silicon		DRIE		Plastic 1		Plastic 2	
SEM source data: (A) No. of channels measured; (B) No. of channels per sample	A	B	A	B	A	B	A	B	A	B
Channels measured	22	22	20	61	22	22	22	22	22	22
Average CSA (mm^2)	0.1263		0.0218		0.1008		0.0728		0.0777	
Sample standard deviation (mm^2)	0.00525		0.00223		0.00152		0.01791		0.01040	
% Deviation (95% CI)	±8.31%		±20.47%		±3.01%		±49.17%		±26.78%	

Table 3 Comparison between SEM measurement of a channel and CAD model created from the SEM photograph of the same channel

Manufacturing method	Wet etched (trapezoidal)	Diced silicon	DRIE	Plastic 1	Plastic 2
Idealized CSA from SEM (mm^2)	0.126878	0.021827	0.102701	0.077563	0.100015
Actual CSA from CAD Model (mm^2)	0.131198	0.019002	0.100054	0.075792	0.093405
% Change	+3.41%	−12.94%	−2.58%	−2.28%	−6.61%

A more important measure of the usefulness of a process is the size repeatability from channel to channel in the one sample. This has been measured in Table 2. Note that all the channels in each sample were measured except for the diced silicon. Because of the small size of the channels produced, the silicon dicing process had 61 channels across a 16 mm width, so every third channel was measured.

The sample standard deviation was used to calculate the average variation between channel sizes. The results presented here are for the standard deviation in the cross-sectional area of each channel. Standard deviations of the channel width and height measurements were similar to each other in all channels except for the channels in plastic 2, where the height deviation is almost three times the width. With all other channels, the height and width deviation are within a factor of two of each other. The CSA measurement can be considered a reasonable representation of the overall variation in the height and width in each channel.

The results in Table 2 show that the DRIE channels are by far the most consistent in size from channel to channel, with 95% percent of them within 3% of the average CSA. This is followed by the wet etched channels of which 95% fall within 8.3% of the average. The diced channels perform far more poorly than this, with the diced silicon being the best, needing a 20.5% size variation to remain within the 95% confidence interval. The channels cut in plastic 1 are the worst performers, varying by over 49%.

Repeatability in an array of channels is essential in order that the flow in each channel is uniform. If there are significant changes in the channel dimensions or blockage in a channel used for cooling, a hot spot will quickly develop.

The main cause of the limited repeatability in the diced plastic channels is contamination in the channels due to the wax used in the sample mounting process. Changing this process will improve the accuracy of these channels. The problems that arise in the plastic channels will not really arise in a mass production situation because either injection molding or embossing will be used to form the channels. This gives added advantages over the dicing saw in that the saw is limited to single straight cuts the full length of the channel area, while molding or embossing will allow far more complex geometry to be formed.

The final calculation performed on the channels is to compare the vertical and horizontal dimensions recorded for individual channels with CAD models built from points measured from the SEM photographs. These measurements will give an approximate measurement of how far off the actual channel cross-section is from the idealized cross-section measured directly using the SEM. For this test, the closer the percent deviation is to zero, the more accurate is the assumption that the channel is a perfect rectangle or trapezium. The DRIE channel is the closest to a perfect rectangle and has the lowest variation in the overall dimensions of the channels. The diced silicon channels are the only ones that very significantly deviate from the target shape, with just short of a 13% difference in area between the idealized rectangular shape of the channel and its actual shape. This value will be used in Part two of this paper to adjust the theoretical flow curve for each channel, improving the theoretical prediction accuracy.

CONCLUSIONS

Dicing processes, though cheap and quite fast, appear to have relatively low repeatability and suffer from contamination problems due to both chipping caused by the cutting process itself and leftover wax from the mounting process required to hold the plastic samples in place during dicing.

Dicing processes are quite limited in the geometry they can produce and are therefore unsuitable for microchannel mass production, especially when compared to embossing and injection molding processes for plastics. Dicing is excellent for quick prototyping of straight channels.

Wet etching, because of its dependence on the crystal orientation in the wafer, is the most complex process used here for making channels in terms of the number of steps required. It does, however, produce accurate and repeatable channels.

The acute angled corners in the wet etched channels allow water to draw itself through the channels using capillary forces. This property should make them ideal candidates for use as microheat pipes. They operate by using capillary forces to draw the liquid phase of the coolant along the corners of the pipe from the condenser to the evaporator end of the pipe. As the coolant evaporates, it returns to the condenser through the center of the pipe.

The DRIE channels are by far the most accurate in terms of their rectangular geometry, their repeatability from channel to channel, and the ability to consistently reach a target depth in the etch.

DRIE isn't limited to crystal planes and so is almost as flexible in creating geometry as embossing or injection molding. It also offers the potential to create a heat sink on the same silicon as the semiconductor device it cools, eliminating junction resistances while conduction resistance is minimized.

Anodic bonding of glass and silicon is a reliable means of joining silicon and glass, but it is a very slow process due to the cleaning necessary before bonding can take place.

NOMENCLATURE

(abc)	Miller index for first plane
D_h	hydraulic diameter, m
P_L	pressure loss through channel, Pa
(xyz)	Miller index for second plane

Greek Symbols

θ	angle between two crystal planes, °

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