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DIRECT COMPARISON BETWEEN A VARIETY OF MICROCHANNELS PART 1: CHANNEL MANUFACTURE AND MEASUREMENT

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ABSTRACT

This paper is the first part of a two part study into the pressure-flow characteristics of a range of microchannels measured over a range of typical Reynolds numbers. Here the manufacture of the channels and their resulting quality is addressed. The target application is silicon cooling.

Wet Etching, Deep Reactive Ion Etching (DRIE) and Precision Sawing have been used to create microchannels in silicon and thermoset plastic. Anodic bonding has been used to bond covers onto the DRIE and Wet Etched channels. Wet etching a (100) silicon wafer using a KOH solution produced trapezoidal channels of width 577µm and height 413µm. DRIE using the Bosch process produced rectangular channels in (100) silicon of width 304µm and height 332µm. Mechanical sawing using a Disco Dicing Saw produced near rectangular channels in both silicon and plastic. The silicon channels were 52µm wide and 423µm deep, and the plastic channels were 203µm wide by 344 or 382µm deep. Channel dimensions were measured using a scanning electron microscope.

Silicon was the main material chosen, since it is possible to cut cooling channels directly into one side of a silicon device, while the electronic parts are deposited on the other, giving effective cooling with minimal thermal resistance. The plastics chosen are commonly used to encapsulate electronic packages and will also be in close proximity to the heat producing regions of the device it protects. Embossed channels on a plastic encapsulant also potentially offer a low cost mass producible means of cooling electronic devices with a low overall thermal resistance. A glass cover was anodically bonded over the silicon channels to prevent channel to channel leakage and provide optical access. The plastic channels were also covered by a glass slide, bonded in position using SU8 Photoresist spun on the glass.

This paper demonstrates the feasibility of producing relatively large microchannels in two materials by three methods. Part two of this paper will describe the modular flow test system and analyze the flow friction through the channels.

NOMENCLATURE

Symbol	Description	Unit
	Roman Symbols	
D_h	Hydraulic Diameter	m
P_L	Pressure Loss Through Channel	Pa
(abc)	Miller Index for First plane	No Unit
(xyz)	Miller Index for Second plane	No Unit
	Greek Symbols	
θ	Angle between two Crystal Planes	°

INTRODUCTION

The sustained drive towards faster, smaller and more complex silicon devices has led to a considerable increase in the power density of modern processor chips. At present cost performance/high performance devices cannot operate reliably at junction temperatures greater than 90°C (ITRS 2003). The International Technology Roadmap for Semiconductors (2003) also predicts this figure to drop to 85°C by 2005. The maximum ambient temperature at which these devices should reliably operate is 45°C, giving a mere 40°C temperature drop across which 80W must be dissipated. These requirements necessitate the design of cooling systems with higher heat transfer coefficients and lower thermal resistances than are currently available. To put this in perspective, the ITRS (2003) states that the power density of the processor chip in a modern computer is

570 000W/m^2. In comparison, a space shuttle can experience heat fluxes of 80 000 W/m^2 during reentry. The power density in silicon processors is predicted to increase by an average of 6% per year until at least 2009 (ITRS 2003).

The use of microchannels to cool silicon devices was first proposed in a paper by Tuckerman and Pease (1981) using wet etched silicon channels. Since then other methods have been used including DRIE (Perret et al, 2000), Electroplating (Joo et al 1995), Precision Sawing (Kishimoto and Sasaki 1987), Electro-discharge Machining (Adams et al 1999), CNC Milling (Yuan et al 2000) and LASER ablation (Hahn et al 1997). The purpose of this study is to make channels using a number of these methods and to rate the suitability of these methods for manufacture and performance as part of a silicon device. Part 2 of this paper will be devoted to describing the test system and measuring the flow through the manufactured channels.

The aim of the manufacturing work described here is to produce a variety of comparable microchannels using diverse methods. In order to allow the channels to be compared, all the channels are cut into the surface of 16 × 30mm rectangular pieces. Since the area of each piece is the same, a test system can be built which uses the same inlet and outlet manifolds, as well as the same data acquisition system to test each channel.

It was decided that if possible all the channels should have a glass cover bonded over them in order to allow optical access to the channels so trapped air bubbles or other unexpected blockages can be spotted. Bonding a cover over the channels also ensures that no flow can pass over the tops of the channel walls. Some theoretical work has shown that leaving a gap over the walls increases the heat transfer from microchannels under constant pumping power (Min et al 2004), but practical control of this gap is difficult.

The manufacturing methods used were developed and carried out in the NMRC, Ireland. The processes used were precision sawing of plastic, silicon and glass, DRIE and KOH Etching.

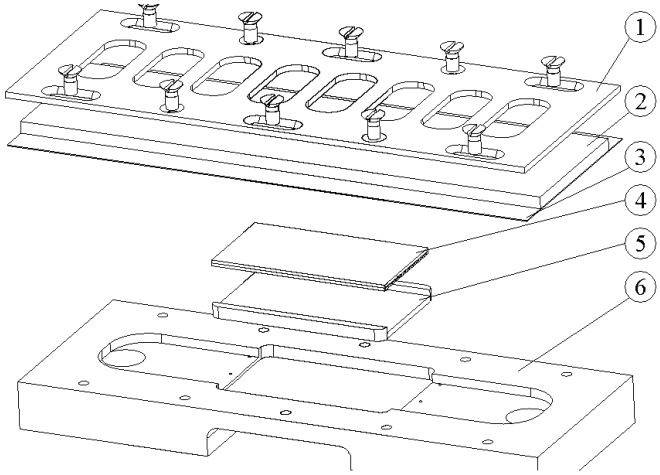

Figure 1: Layout of the Microchannel Tester.

The experimental apparatus that has been made to test these samples uses the same inlet and outlet manifolds, pressure tappings and thermocouples to test each channel. It is built using as many standard parts as possible, allowing it to be dismantled and rebuilt easily as well as allowing the whole system to be rearranged if necessary.

As can be seen from Figure 1, the sample (4) fits into the shim (5), which then fits into the manifold block (6). Because the samples are available in a variety of thicknesses, several shims have been made with different depth grooves. The result of this is that all the channel samples, when fitted in their corresponding shims, occupy the same volume. Since the only change in the flow system from sample to sample is the size of the channels being tested, the effects of different manifolds, pressure tapping locations and thermocouple locations are eliminated even though totally different channels are being tested.

PLASTIC MANUFACTURING PROCESS

The plastic channels were made from two different thermoset plastics. These are known by the names Nitto PMC and Plascon PMC. Since both are used in the encapsulation of silicon devices, it makes sense to investigate their thermal performance as channels could potentially be embossed onto the chip encapsulation far more cheaply and easily than they could be etched into the silicon chip and with a lower thermal resistance than a heat sink clamped onto the encapsulated chip.

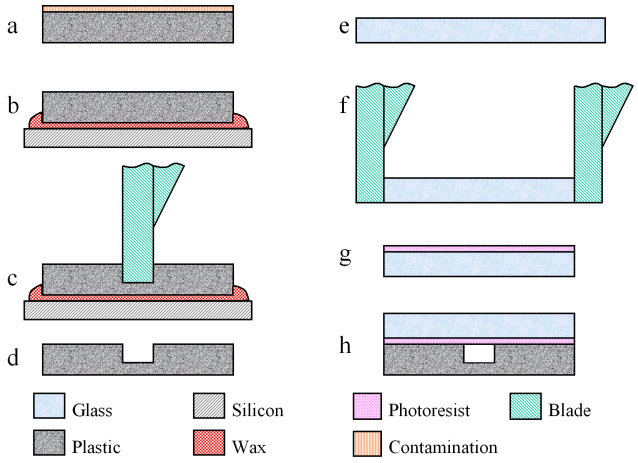

Figure 2: Processing Steps in the manufacture of plastic channels

The plastic samples were made by injecting plastic into an empty 35mm BGA mould causing contamination to be left on the sample (See Figure 2 (a)). This is removed with light emery paper. The sample was then mounted on a silicon wafer using wax (b). This allows a standard vacuum chuck to hold the sample in position during cutting.

The dicing saw used is a Disco Automatic dicing saw DAD-2H/6T. Prior to use, the saw calibrates itself by touching the blade off the chuck on which the sample sits. This allows wear in the blade and different blade diameters to be compensated for and gives a zero from which the cutting depth can be set.

Cutting was performed using a plastic specific blade. A thin layer of spray paint had to be applied to the surface of

the sample in order to allow the optical alignment of the sample with the blade to take place.

After cutting the remaining paint was polished off the surface of the sample using a Logitech PM2 Precision Polishing Machine and 3 micron diamond paste. This leaves a clean flat surface for the glass to be bonded over. Any remaining wax from the mounting process is melted off on a hotplate or dissolved in an acetone bath at 70°C.

A 100mm (4") glass wafer is diced into pieces the same size as the plastic samples using a resin bonded diamond blade (f). A layer of photoresist is spun over the glass (g). SU8-5 is the resist used. This is an epoxy based negative photoresist that can be cured under UV light.

The glass and plastic are heated to 70°C on a hot plate. The glass pieces are then aligned and pressed into position over the plastic samples. Point pressure is applied by rolling a clock glass over the surface of the glass to create an initial bond. The partially bonded samples are then exposed to UV light. This starts a crosslinking process in the SU8. Heating the sample to 95°C and holding it at that temperature for 5 minutes completes the crosslinking, bonding the plastic to the glass (h).

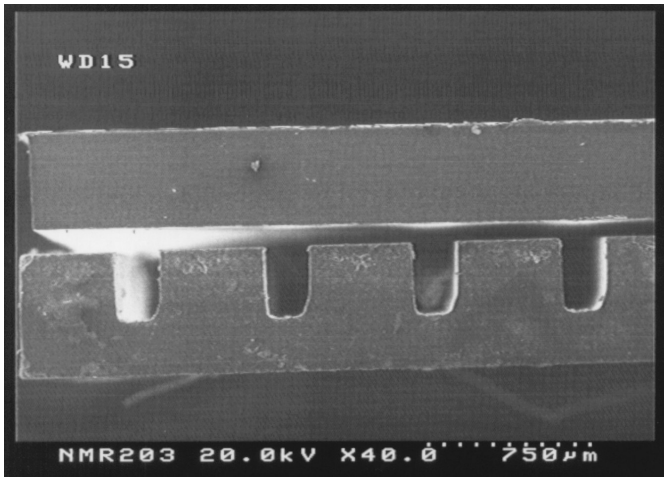

Figure 3: Nitto Plastic channels with glass cover. The gap between the plastic and glass is due to warping in the plastic. SU8 is used to bond the glass to the plastic.

Several problems were evident in this process. The first was that accurate control of the channel depth was extremely difficult due to the difficulty in controlling the thickness of the wax bed holding the sample in position during sawing. The second problem was due to the plastic samples being slightly warped, preventing adequate contact for the bond between the plastic and the glass to be successful over the entire area of the sample. This warping wasn't noticed initially because in order to mount the sample in a wax bed, a weight was placed over the sample while the wax was still molten, holding the sample flat while it was mounted in wax.

Since the sample is clamped in position on the flow test apparatus (Figure 1), this gap will be reduced, so the overall effect of the gap on flow results should be less significant. The warping in the samples is most likely a side effect of the curing process needed to crosslink the plastic samples after they have been molded. Using thermoplastics would remove this problem and also make the embossing process much easier. Thermoset plastics tend to have higher thermal conductivities than thermoplastics due to their higher crystallinity, but actual conductivities are still in the region of 500 times less than that of silicon.

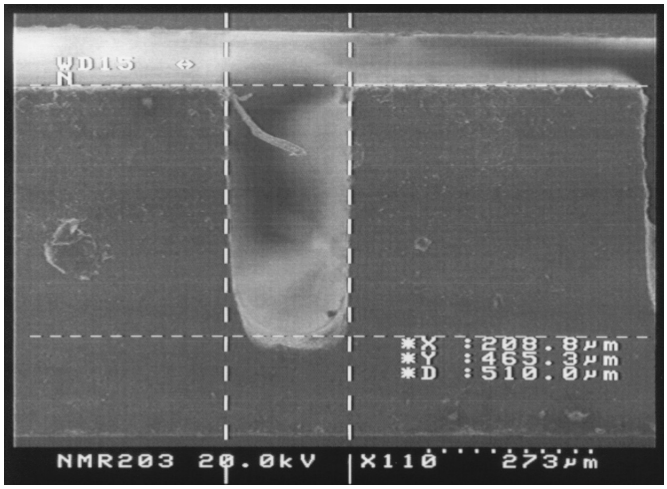

Figure 4: Plascon Plastic channel. This is cut with the same blade as the Nitto Channel but is slightly deeper.

ANODIC BONDING

Anodic bonding is a process that allows silicon and glass to be irreversibly bonded. The glass being used must contain a significant amount of Sodium (Na) in order for the bonding to be successful. Pyrex fulfills this requirement and was used for all the processes described here.

For silicon and glass to be bonded their surfaces must be perfectly clean. Cleaning was performed by first boiling both wafers in Isopropyl Alcohol, dipping the silicon wafer in a 10:1 Deionised (DI) water, Hydrofluoric Acid solution for 10 seconds and then cleaning all wafers in a solution of H_2O_2, NH_4OH and DI water in a 1:1:5 Ratio, followed by a solution of H_2O_2, HCl and DI water in a 1:1:5 Ratio. The wafers are then boiled in methanol and baked at 160°C to ensure the wafer surfaces are dry.

The wafers were placed in a furnace at 400°C, for 2 hours. An electrical current was then applied between the silicon and the glass for 5 hours to create the bond. The completeness of the bond can be determined by visually inspecting the wafer, as the bonded areas are clearly visible through the glass.

In order for the bond to propagate easily from where it starts below the electrode at the center of the glass wafer to the edges of the wafer there must be a continuous contact surface along which the bond can travel. If there are islands of silicon on the wafer they may not bond. This consideration was essential in the mask design.

By controlling the atmosphere in the furnace where the bonding takes place, it may also be possible for example, to combine the process of bonding the wafers with other processes such as charging heat pipes.

SILICON MANUFACTURING – DICING SAW

The dicing saw was also used to cut channels a silicon wafer. This was much more straightforward than the plastic process as the wafer can be mounted directly to the dicing saw vacuum chuck. Control of the depth of the channels was far easier for this process compared to the plastic dicing because there was no wax layer needed to hold the sample in place. A standard silicon specific dicing blade was used for this cutting, creating channels approximately 50×440µm in size. These are shown in Figure 5.

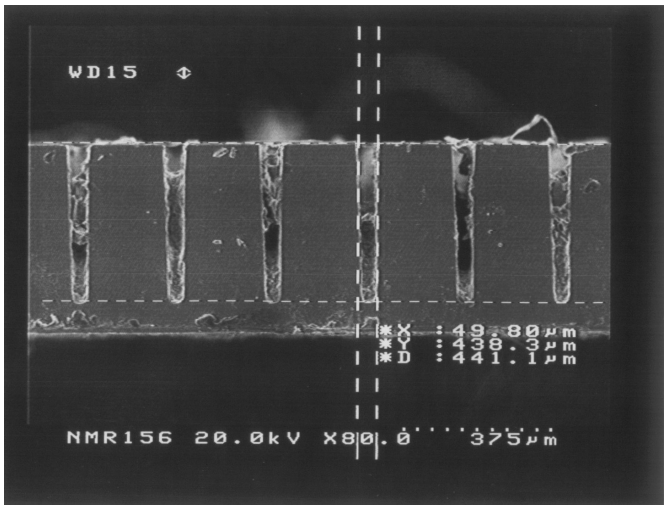

Figure 5: Diced silicon wafer. Contamination is due to handling outside clean room environments and chips remaining from the dicing process.

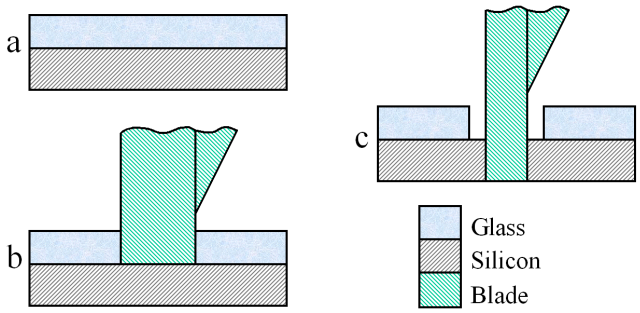

Figure 6: Two step dicing process.

The dicing saw was also used to cut all the other silicon wafers into 16×30mm samples in order that they could be flow tested. To the author's knowledge no dicing saw blades are available capable of cutting both silicon and glass at once. Because of this a two-step cutting procedure was needed as shown in Figure 6.

Two different blades were used; the first was a 200µm wide blade that cut through the glass wafer (b). A second 100µm wide blade was then used which cut into the floor of the previous cut to completely separate each sample from the rest of the wafer (c).

SILICON MANUFACTURING - DRIE

Deep reactive Ion Etching (DRIE) is a process that uses gas rather than liquid to etch features into a silicon substrate. DRIE is anisotropic, so the crystal orientation of the wafer isn't important to the accuracy of the features created.

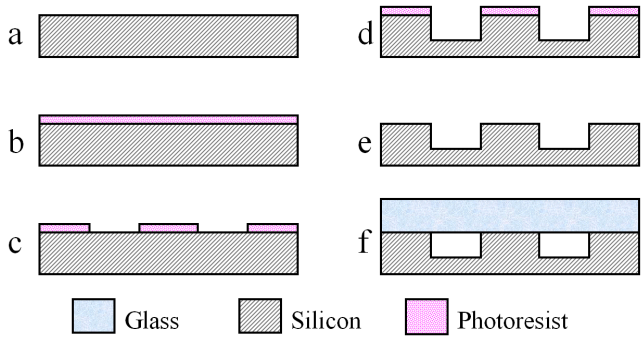

Figure 7: DRIE Process including anodic bonding of a glass wafer onto the etched silicon.

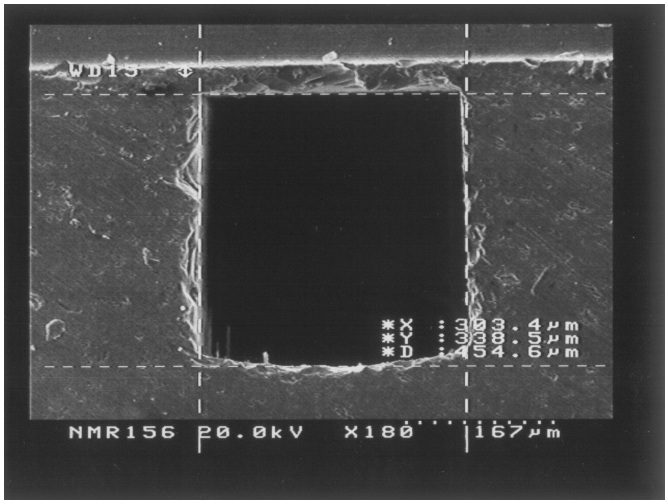

Figure 8: DRIE Channel. Damage visible around the channel and the step in the glass over the channel are due to the Dicing process.

The Bosch process was used to produce near vertical channel walls. This process works by first etching the silicon anisotropically for a short distance. The silicon is then coated with an etch inhibitor which is only removed from the bottom of the channel during the next etch. By alternating these steps high aspect ratio trenches with near vertical walls can be produced.

The DRIE process used for this work (Figure 7) begins by spinning a layer of positive photoresist (SPR 220) on the wafer (b). This is patterned using a glass mask. The resist is then developed, transferring the pattern from the mask to the resist (c). Areas covered by the resist are not etched.

The etching process then begins (d). Initially a 400µm depth was aimed for, but at this depth the wafer became too brittle to be safely handled in the cleaning steps after etching. The photoresist also began to break down at this depth, reducing the accuracy with which the pattern was etched into the silicon. After etching the resist is removed (e) and a glass wafer is anodically bonded over the channels

(f). Figure 8 shows a Scanning Electron Microscope (SEM) picture of a DRIE channel with a bonded glass cover.

SILICON MANUFACTURING - KOH ETCHING

Potassium Hydroxide (KOH) etching was also used to etch channels into a 100mm (100) silicon wafer. KOH etches through (100) planes approximately 30 times as quickly as (111) planes. This results in trapezoidal or triangular channels depending on the etch duration. The wall angle of the channels can be calculated using Equation (1) where the Miller Indices of the planes are (abc) and (xyz). For the KOH etch described here the wall angle is 54.74°.

$$\theta = Cos^{-1}\left(\frac{ax+by+cz}{\sqrt{a^2+b^2+c^2}\times\sqrt{x^2+y^2+z^2}}\right) \qquad \textbf{(1)}$$

Since the etch stops at the (111) planes in the silicon, a misalignment between the details on the mask and the (111) planes will produce stepped channel walls. For this reason, an alignment etch as described by Ensell (1996) must be used. This etch uses a mask with 50µm diameter circular holes that etch silicon in KOH to form pyramid shaped pits. The sloped walls of these pits follow the (111) planes in the wafer, allowing the channel mask to be correctly aligned.

The wet etch process (Figure 9) begins with a wafer clean and the growth of furnace oxide on the surface of the wafer (b). A chemical vapor deposited nitride layer, resistant to the KOH solution, is deposited over the oxide (c). Photoresist is spun over the nitride layer and patterned using the alignment mask (d, e).

After the resist has been developed, a plasma etch is used to remove the exposed nitride (f). The photoresist is then removed (g). A Sulphuric Acid bath is used to remove the exposed oxide (h) and the alignment marks are KOH etched to a depth of 14 microns (i).

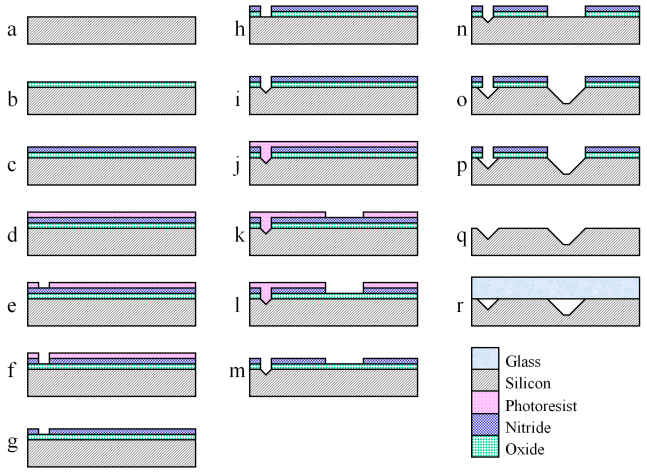

Figure 9: Wet etching process. Note the use of the same oxide and nitride layers for both etches in order to reduce the number of process steps.

The etch marks are then inspected, new resist is spun over the surface of the wafer (j) and the mask with the channel details is placed over it and aligned to the etching marks already on the wafer. The etching process as described in the previous paragraph is then repeated producing etched microchannels (k-p). Etch depth is controlled by carefully measuring the etch duration as the etch rate is already known. The oxide and nitride are then removed (q). Finally a glass wafer is anodically bonded over the silicon wafer (r) and the wafer is diced using the two-step process. The resulting channel can be seen in Figure 10.

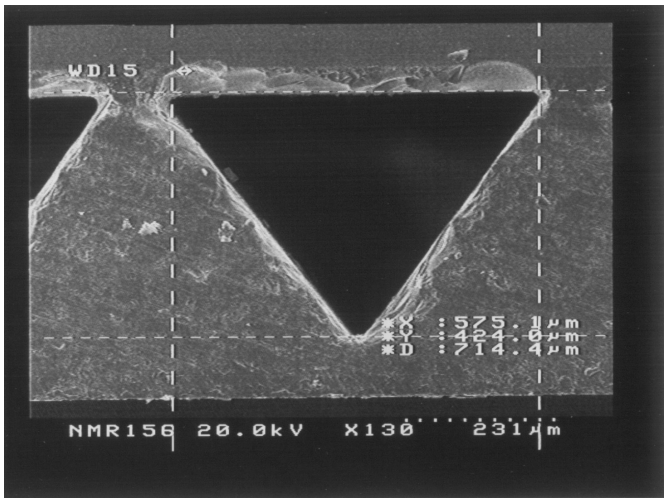

Figure 10: Wet etched trapezoidal channel with anodically bonded pyrex cover. Etch was stopped when Channel was just short of being triangular.

CHANNEL MEASUREMENTS

The most significant source of error in matching the theoretical performance of channels with their experimental performance is that of measuring the size of the channel. This is why careful measurement of the dimensions of the channels is fundamental to correlating theoretical calculations for both pressure drop and heat transfer with measurements made.

Equation (2) shows the relationship between the pressure drop and the hydraulic diameter for a constant channel length and mass flow rate. The reason that the measurement of the channels is critical is because a small change in D_h will lead to significant changes in the pressure drop due to the high power to which D_h is raised.

$$P_L \propto \frac{1}{D_h^{\,4}} \qquad \textbf{(2)}$$

The channels were measured using a scanning electron microscope (SEM), calibrated monthly to ±0.3µm on a 10µm measurement. This allowed direct vertical and horizontal measurements to be made on the channels and produced photographs of the channels.

A program called DataThief was then used to take scaled points from the SEM pictures (See Figure 11). These points were exported as text to ProEngineer, a CAD program, where they were used to create a 3D model of the channel cross section. By analyzing the model, a more

accurate measure of the cross sectional area and hydraulic diameter of the channel were calculated.

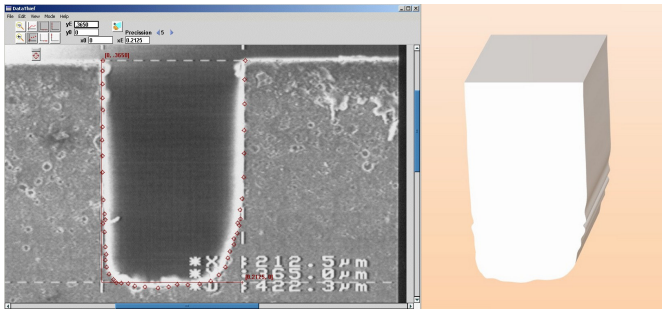

Figure 11: SEM Photograph of a Nitto plastic channel with overlaid data points on left, CAD model of channel made using these points on right.

It should be noted that since the cross section of the channel can't be assumed to be constant along it's length, the measurements taken above only allow a comparison to be made between the accuracy of the overall width and height for an idealized rectangular channel as measured by the SEM and a more accurate model of the channel made from points taken from the same picture. Channel measurements were only taken through one plane for each sample.

RESULTS

The following page contains a summary of the results recorded. Table 1 contains a comparison between the target dimensions of the channels for each manufacturing method and the actual dimensions measured for each process.

Table 2 contains the averaged dimensions of each channel, the number of channels measured in each sample and the sample standard deviation of the measured channel sizes for each process. Every third channel was measured on the diced silicon samples and all channels were measured for the other four samples.

Table 3 compares the results from single channels, which are assumed to be perfectly rectangular or trapezoidal, with a CAD model of the actual cross section of the particular channel from a SEM photograph. The measurements that assume the channel to be perfectly rectangular or trapezoidal go towards the average dimensions in Table 2.

DISCUSSION

The data in Table 1 compares the expected dimensions for each channel with the actual dimensions measured for each channel. It can be seen that all processes are well within 10% of the target dimensions in terms of cross sectional area (CSA).

For both the wet etch and DRIE processes, there was no way to check the depth of the channels while they were being processed as the depth is a function of the etch time. The features etched using these processes are deeper than most of the etches performed in the NMRC, so its understandable that the estimates of depth were slightly out. Both processes still produce channels that only deviate 5% from the target channel size.

For the dicing processes changing the blade height in the saw controls the cutting depth. The error in the final depth of the diced silicon channels is most likely due to either the plastic film on which the wafer is stuck being thicker than expected or vibration in the blade as it cuts. The silicon wafer thickness was measured with a micrometer to be 525±1µm thick. This is equal to the supplier's quoted thickness.

There was far more variation evident in the depth in the diced plastic samples. This is due to a lack of repeatability in controlling the thickness of the wax layer between the silicon wafer and the plastic sample. Both the Nitto and Plascon samples were intended to have the same dimensions, but instead there's a difference of almost 40µm in their depths.

The 2.87% correlation between the target channel size and the actual size of the Plascon channels (See Table 1) is not an indication that the process is repeatable. Separate test cuts, intended to be 600µm deep in another Plascon sample turned out to be 439µm deep instead, showing the level of variation potentially present in the process. All the diced channels tested here are 2 or 3 microns wider than the nominal size of the blades used to cut them. This difference is likely to be the contribution of vibration to the width variation in the channels.

A more important measure of the usefulness of a process is the size repeatability from channel to channel in the one sample. This has been measured in Table 2. Note that all the channels in each sample were measured except for the diced silicon. The silicon dicing process, because of the small size of the channels produced, had 61 channels across a 16mm width, so every third channel was measured.

The sample standard deviation was used to calculate the average variation between channel sizes. The results presented here are for the standard deviation in the cross sectional area of each channel. Standard deviations of the channel width and height measurements were similar enough to each other in all channels except the Plascon channels where the height deviation is almost three times the width. With all other channels the height and width deviation are within a factor of 2 of each other. The CSA measurement can be considered a reasonable representation of the overall variation in height and width in each channel.

The results in Table 2 show that the DRIE channels are by far the most consistent in size from channel to channel with 95% percent of them within 3% of the average CSA. This is followed by the wet etched channels of which 95% fall within 8.3% of the average. The diced channels perform far more poorly than this with the diced silicon being the best needing a 20.5% size variation to remain within the 95% confidence interval. The Nitto plastic channels are the worst performers, varying by over 49%.

Repeatability in an array of channels is essential in order that the flow in each channel is uniform. If there are significant changes in the channel dimensions or there is blockage in a channel used for cooling a hot spot will quickly develop.

Table 1: Comparison between the Target channel dimensions and the actual dimensions produced by each process.

Process Target Vs. Manufactured Channel Size	Manufacturing Method	Wet Etched (Trapezoidal)		Diced Silicon		DRIE		Nitto Plastic		Plascon Plastic	
		Target	**Actual**	**Target**	**Actual**	**Target**	**Actual**	**Target**	**Actual**	**Target**	**Actual**
	Width (mm)	0.585	0.577	0.05	0.052	0.3	0.304	0.2	0.202	0.2	0.203
	Height (mm)	0.4	0.413	0.4	0.423	0.32	0.332	0.4	0.344	0.4	0.382
	CSA (mm^2)	0.1209	0.126	0.0200	0.022	0.0960	0.101	0.0800	0.073	0.0800	0.078
	% Difference Width|Height	**-3.25%**	**+1.37%**	**-5.75%**	**-4.00%**	**-3.75%**	**-1.33%**	**+14.0%**	**-1.00%**	**+4.50%**	**-1.50%**
	% Difference CSA	**+4.50%**		**+9.07%**		**+5.04%**		**-8.95%**		**-2.87%**	

Table 2: SEM Measurements of 5 Sets of Microchannels. (95% Confidence Interval (CI) = Average Value ± 2×Sample Standard Deviation)

Size Comparison between channels on the same sample. A low Percent Deviation means all Channels are similar in size indicating that the Process is Consistent	Manufacturing Method	Wet Etched (Trapezoidal)		Diced Silicon		DRIE		Nitto Plastic		Plascon Plastic	
	SEM SOURCE DATA: (A) No. OF CHANNELS MEASURED (B) No. OF CHANNELS PER SAMPLE	**A**	**B**	**A**	**B**	**A**	**B**	**A**	**B**	**A**	**B**
	Channels Measured	22	22	20	61	22	22	22	22	22	22
	Average CSA (mm^2)	0.1263		0.0218		0.1008		0.0728		0.0777	
	Sample Standard Deviation (mm^2)	0.00525		0.00223		0.00152		0.01791		0.01040	
	% Deviation (95% CI)	**±8.31%**		**±20.47%**		**±3.01%**		**±49.17%**		**±26.78%**	

Table 3: Comparison between SEM measurement of a channel and CAD model created from the SEM photograph of the same channel.

Measure of correlation between the Idealized channel shape and the actual (CAD) channel shape	Manufacturing Method	Wet Etched (Trapezoidal)	Diced Silicon	DRIE	Nitto Plastic	Plascon Plastic
	Idealized CSA from SEM (mm^2)	0.126878	0.021827	0.102701	0.077563	0.100015
	Actual CSA from CAD Model (mm^2)	0.131198	0.019002	0.100054	0.075792	0.093405
	% Change	**+3.41%**	**-12.94%**	**-2.58%**	**-2.28%**	**-6.61%**

The main cause of the limited repeatability in the diced plastic channels is contamination in the channels due to the wax used in the sample mounting process. Changing this process will improve the accuracy of these channels. The problems that arise in the plastic channels will not really arise in a mass production situation because either injection molding or embossing will be used to form the channels. This gives added advantages over the dicing saw in that the saw is limited to single straight cuts the full length of the channel area while molding or embossing will allow far more complex geometry to be formed.

The final calculation performed on the channels is to compare the vertical and horizontal dimensions recorded for individual channels with CAD models built from points measured from the SEM photographs. These measurements will give an approximate measurement of how far off the actual channel cross section is from the idealized cross section measured directly using the SEM. For this test the closer the percent deviation is to zero the more accurate is the assumption that the channel is a perfect rectangle or trapezium. The DRIE channel is the closest to a perfect rectangle and also has the lowest variation in the overall dimensions of the channels. The diced silicon channels are the only ones that very significantly deviate from the target shape with just short of a 13% difference in area between the idealized rectangular shape of the channel and its actual shape. This value will be used in Part 2 of this paper to adjust the theoretical flow curve for each channel, improving the theoretical prediction accuracy.

CONCLUSIONS

Dicing processes, though cheap and quite fast appear to have relatively low repeatability and suffer from contamination problems due to both chipping caused by the cutting process itself and left over wax from the mounting process required to hold the plastic samples in place during dicing.

Dicing processes are quite limited in the geometry they can produce and therefore unsuitable for microchannel mass production, especially when compared to embossing and injection molding processes for plastics.

Dicing is excellent for quick prototyping of straight channels.

Wet etching, because of its dependence on the crystal orientation in the wafer, is the most complex process used here for making channels in terms of the number of steps required. It does however produce accurate and repeatable channels.

The acute angled corners in the wet etched channels allow water to draw itself through the channels using capillary forces. This property should make them ideal candidates for use as micro heat pipes. These operate by using capillary forces to draw the liquid phase of the coolant along the corners of the pipe from the condenser to the evaporator end of the pipe. As the coolant evaporates it returns to the condenser through the center of the pipe.

The DRIE channels are by far the most accurate in terms of their rectangular geometry, their repeatability from channel to channel and the ability to consistently reach a target depth in the etch.

DRIE isn't limited to crystal planes and so is almost as flexible in creating geometry as embossing or injection molding. It also offers the potential to create a heat sink on the same silicon as the semiconductor device it cools, eliminating junction resistances while conduction resistance is minimized.

Anodic bonding of glass and silicon is a reliable means of joining silicon and glass, but it is a very slow process due to the cleaning necessary before bonding can take place.

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REFERENCES

1. Adams, T. M.; Dowling, M. F.; Abdel-Khalik, S. I. and Jeter, S. M.; Applicability of traditional turbulent single-phase forced convection correlations to non-circular microchannels, *International Journal of Heat and Mass Transfer, Volume 42, Issue 23, December 1999, Pages 4411-4415*

2. Ensell, G., Alignment of mask patterns to crystal orientation, *Sensors and Actuators A 53. (1996) 345-348*

3. Hahn, R.; Kamp, A.; Ginolas, A.; Schmidt, M.; Wolf, J.; Glaw, V.; Toepper, M.; Ehrmann, O.; Reichl H., High power multichip modules employing the planar embedding technique and microchannel water heat sinks, *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A, Volume: 20 Issue: 4 , Dec. 1997 Page(s): 432 –441*

4. International Technology Roadmap for Semiconductors 2003 Edition, *"Assembly and Packaging", 2003* *http://public.itrs.net/Files/2003ITRS/Home2003.htm*

5. Joo, Youngcheol; Dieu, Kiet; Kim, Chang-Jin; Fabrication of monolithic microchannels for IC chip cooling, *MEMS '95, Proceedings. IEEE, 1995 Page(s): 362*

6. Kishimoto T., Sasaki S., Cooling characteristics of diamond-shaped interrupted cooling fin for high power LSI devices, *Electronics Letters, Vol 23, pp. 456-457, 1987*

7. Min, Jung Yim; Jang, Seok Pil and Kim, Sung Jin; Effect of tip clearance on the cooling performance of a microchannel heat sink, *International Journal of Heat and Mass Transfer, Volume 47, Issue 5, February 2004, Pages 1099-1103*

8. Perret, C.; Boussey, J.; Schaeffer, C.; Coyaud, M., Analytic modeling, optimization, and realization of cooling devices in silicon technology, *IEEE Transactions on Components, Packaging and Manufacturing Technology, Part A: Packaging Technologies, Volume: 23 Issue: 4, Dec. 2000 Page(s): 665 -672*

9. Tuckerman, D. B. and Pease, R. F. W., High performance heat sinking for VLSI, *IEEE Electronic Device Letters, Volume EDL 2, Pages 126-129, May 1981*

10. Yuan, Lang; Joshi, Yogendra K.; Nakayama, Wataru; Effect of condenser location and imposed circulation on the performance of a compact two-phase thermosyphon for high power LSI devices, *Engineering Foundation Conference on Heat Transfer and Transport Phenomena for Microsystems, Banff, Alberta, Canada, October 15-20, 2000, pp. 304-311, Electronics Letters, Vol 23, pp. 456-457, 1987*